TEST REPORT
IEEE 1547
IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems

Report Number..... :	230726009GZU-001
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Total number of pages	36 pages
Name of Testing Laboratory preparing the Report.....:	Intertek Testing Services Shenzhen Ltd. Guangzhou Branch Room 02, & 101/E201/E301/E401/E501/E601/E701/E801 of Room 01 1-8/F., No. 7-2. Caipin Road, Science City, GETDD, Guangzhou, Guangdong, China
Applicant's name.....:	Huawei Digital Power Technologies Co., Ltd.
Address .....:	Office 01, 39th Floor, Block A, Antuoshan Headquarters Towers, 33 Antuoshan 6th Road, Futian District, Shenzhen, 518043, P.R.C.
Test specification:	
Standard :	IEEE 1547: 2003, IEEE 1547a:2014 & IEEE 1547.1: 2005+ A1: 2015
Test procedure..... :	Type approval
Condition of the item tested :	Prototype
Non-standard test method……..:	N/A
Test Report Form No.....:	IEEE1547_a
Test Report Form(s) Originator.....:	Intertek Testing Services Shenzhen Ltd. Guangzhou Branch
Master TRF .....:	Dated 2021-04

Test item description..... :	SOLAR INVERTER
Trade Mark .....:	HUAWEI
Manufacturer.....:	Same as applicant
Model/Type reference.....:	SUN2000-8K-LC0, SUN2000-10K-LC0

Ratings.....:

Model	SUN2000-8K-LC0	SUN2000-10K-LC0
Max. Input voltage	600V	
MPPT voltage range	40-560V	
Max. MPPT input current	16A*3	
PV Isc	20A*3	
Rated output power	8000W	10000W
Rated Output apparent power	8000VA	10000VA
Nominal output voltage	W/N/PE 220/230/240Vac	
Rated. output current	36.4A/220Vac 34.8A/230Vac 33.3A/240Vac	45.5A/220Vac 43.5A/230Vac 41.7A/240Vac
Max. output current	40A	45.5A
Nominal output frequency	60 Hz	
Battery max. voltage	600Vdc	
Battery voltage range	350-600Vdc	
Battery maximum current	25Adc	
Battery type	Li-ion	
Power factor range	0.8Leading ~ 0.8Lagging	
Safety level	Class I	
Ingress protection	IP66	
Operation ambient temperature	-25℃ - +60℃	
Software version	V100R023	

Responsible Testing Laboratory (as applicable), testing procedure and testing location(s):			
☒	**Testing Laboratory:**	Intertek Testing Services Shenzhen Ltd. Guangzhou Branch	
Testing location/ address ..... :		Room 02, & 101/E201/E301/E401/E501/E601/E701/E801 of Room 01 1-8/F., No. 7-2. Caipin Road, Science City, GETDD, Guangzhou, Guangdong, China	
☐	**Associated CB Testing Laboratory:**	N/A	
Testing location/ address ..... :		N/A	
Tested by (name, function, signature) ..... :		Shawn Liu Project handler	Shawn Liu
Approved by (name, function, signature) .. :		Gaison Li Reviewer	Gaison Li
☐	**Testing procedure: CTF Stage 1:**	N/A	
Testing location/ address ..... :		N/A	
Tested by (name, function, signature) ..... :		N/A	
Approved by (name, function, signature) .. :		N/A	
☐	**Testing procedure: CTF Stage 2:**	N/A	
Testing location/ address ..... :		N/A	
Tested by (name + signature)..... :		N/A	
Witnessed by (name, function, signature) . :		N/A	
Approved by (name, function, signature) .. :		N/A	
☐	**Testing procedure: CTF Stage 3:**	N/A	
☐	**Testing procedure: CTF Stage 4:**	N/A	
Testing location/ address ..... :		N/A	
Tested by (name, function, signature) ..... :		N/A	
Witnessed by (name, function, signature) . :		N/A	
Approved by (name, function, signature) .. :		N/A	
Supervised by (name, function, signature) :		N/A	

List of Attachments (including a total number of pages in each attachment): **N/A**	
Summary of testing:	
Tests performed (name of test and test clause): All applicable tests	**Testing location:** Intertek Testing Services Shenzhen Ltd. Guangzhou Branch Room 02, & 101/E201/E301/E401/E501/E601/E701/E801 of Room 01 1-8/F., No. 7-2. Caipin Road, Science City, GETDD, Guangzhou, Guangdong, China
Summary of compliance with National Differences (List of countries addressed): N/A ☒ **The product fulfils the requirements of** IEEE 1547: 2003 & IEEE 1547.1: 2005+ A1: 2015	

Copy of marking plate:

The artwork below may be only a draft. The use of certification marks on a product must be authorized by the respective NCBs that own these marks.

Note:

1. The above markings are the minimum requirements required by the safety standard. For the final production samples, the additional markings which do not give rise to misunderstanding may be added.
2. Label is attached on the side surface of enclosure and visible after installation.

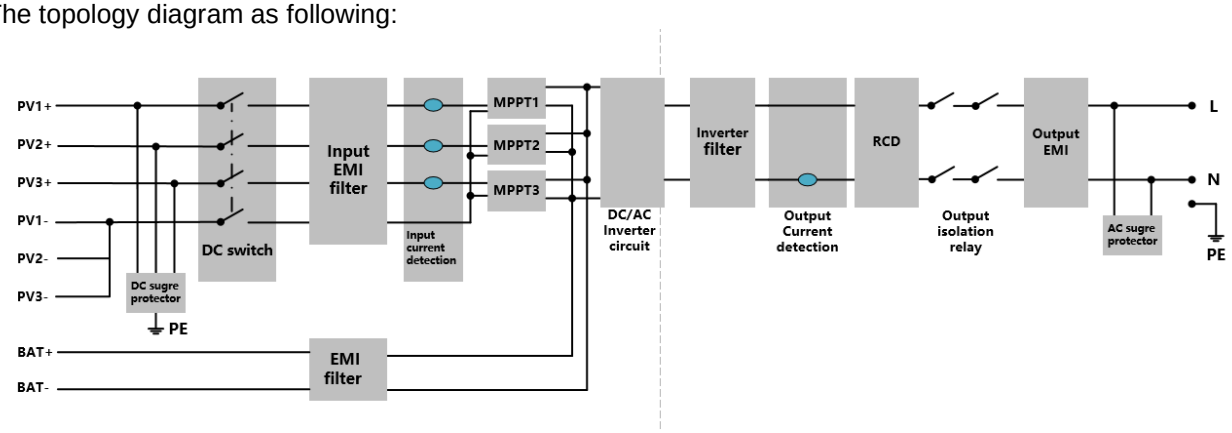
Test item particulars..... :	
Equipment mobility ..... :	☐ movable ☐ hand-held ☐ stationary ☒ fixed ☐ transportable ☐ for building-in
Connection to the mains..... :	☐ pluggable equipment ☐ direct plug-in ☒ permanent connection ☐ for building-in
Environmental category..... :	☒ outdoor ☐ indoor unconditional ☐ indoor conditional
Over voltage category Mains ..... :	☐ OVC I ☐ OVC II ☒ OVC III ☐ OVC IV
Over voltage category DC ..... :	☐ OVC I ☒ OVC II ☐ OVC III ☐ OVC IV
Mains supply tolerance (%)..... :	-90 / +110 %
Tested for power systems..... :	TN systems
IT testing, phase-phase voltage (V)..... :	- - -
Class of equipment..... :	☒ Class I ☐ Class II ☐ Class III ☐ Not classified
Mass of equipment (kg) ..... :	Approx. 17.5Kg
Pollution degree..... :	Outside PD3; Inside PD2
IP protection class..... :	IP 66
..... :	
Possible test case verdicts:	
- test case does not apply to the test object..... :	N/A
- test object does meet the requirement..... :	P (Pass)
- test object was not evaluated for the requirement ..... :	N/E
- test object does not meet the requirement..... :	F (Fail)
Testing..... :	
Date of receipt of test item ..... :	26 July., 2023
Date (s) of performance of tests..... :	27 July., 2023 – 11 Sep., 2023

General remarks:	
"(See Enclosure #)" refers to additional information appended to the report. "(See appended table)" refers to a table appended to the report. **Throughout this report a ☐ comma / ☒ point is used as the decimal separator.**	
Manufacturer's Declaration per sub-clause 4.2.5 of IECEE 02:	
The application for obtaining a CB Test Certificate includes more than one factory location and a declaration from the Manufacturer stating that the sample(s) submitted for evaluation is (are) representative of the products from each factory has been provided ..... :	☐ **Yes** ☒ **Not applicable**
When differences exist; they shall be identified in the General product information section.	
Name and address of factory (ies) ..... :	Liding Electronic Technology (Dongguan) Co., LTD. Building 2, No.313, Qingxi North Ring Road, Qingxi Town, Dongguan City, Guangdong Province, P.R.China.

General product information:

The unit is bidirectional which applies to the PV system with battery storage. Energy produced by the PV system is used to optimize self-consumption. Excess energy is used to charge the batteries, and then fed into the public grid when the PV energy is adequate.

The topology diagram as following:



Model difference:

All models are identical, except model SUN2000-10K-LC0 has an external fan and the output power derating in software.

The product was tested on:

The Software version: V100R023

The Hardware version: V100R023

The reference impedance: Z_source = 1,05 + j 0,32 ohm, I_SC = 210 A

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Clause	Requirement – Test	Result – Remark	Verdict

4.1	**General requirements**		**P**
4.1.1	Voltage regulation		P
	Coordination with and approval of, the area EPS and DR operators, shall be required for the DR to actively participate to regulate the voltage by changes of real and reactive power. The DR shall not cause the Area EPS service voltage at other Local EPSs to go outside the requirements of ANSI C84.1-2011 1995, Range A.	This unit is local electric power system (Local EPS). The unit is complied with specified ANSI C84.1.	P
4.1.2	Integration with Area EPS grounding		N/A
	The grounding scheme of the DR interconnection shall not cause overvoltages that exceed the rating of the equipment connected to the Area EPS and shall not disrupt the coordination of the ground fault protection on the Area EPS.	No DR interconnection.	N/A
4.1.3	Synchronization		P
	The DR unit shall parallel with the Area EPS without causing a voltage fluctuation at the PCC greater than ±5% of the prevailing voltage level of the Area EPS at the PCC,and meet the flicker requirements of 4.3.2.		P
4.1.4	Distributed resources on distribution secondary grid and spot networks		N/A
4.1.4.1	Distribution secondary grid networks		N/A
	This topic is under consideration for future revisions of this standard.		N/A
4.1.4.2	Distribution secondary spot networks		N/A
	Network protectors shall not be used to separate, switch, serve as breaker failure backup or in any manner isolate a network or network primary feeder to which DR is connected from the remainder of the Area EPS,unless the protectors are rated and t ested per applicable standards for such an application.	The unit does not included reclosing of any network protectors installed on the spot network.	N/A
	Any DR installation connected to a spot network shall not cause operation or prevent reclosing of any network protectors installed on the spot network. This coordination shall be accomplished without requiring any changes to prevailing network protector clearing time practices of the Area EPS.		N/A
	Connection of the DR to the Area EPS is only permitted if the Area EPS network bus is already energized by more than 50% of the installed network protectors.		N/A
	The DR output shall not cause any cycling of network protectors.		N/A
	The network equipment loading and fault interrupting capacity shall not be exceeded with the addition of DR.		N/A
	DR installations on a spot network, using an automatic transfer scheme in which load is transferred between the DR and the EPS in a		N/A

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Clause	Requirement – Test	Result – Remark	Verdict
	momentary make-before-break operation, shall meet all the requirements of this clause regardless of the duration of paralleling.		
4.1.5	Inadvertent energization of the Area EPS		P
	The DR shall not energize the Area EPS when the Area EPS is de-energized.		P
4.1.6	Monitoring provisions		N/A
	Each DR unit of 250 kVA or more or DR aggregate of 250 kVA or more at a single PCC shall have provisions for monitoring its connection status, real power output, reactive power output, and voltage at the point of DR connection.	This unit output is less than 250kVA.	N/A
4.1.7	Isolation device		N/A
	When required by the Area EPS operating practices, a readily accessible, lockable, visible-break isolation device shall be located between the Area EPS and the DR unit.		N/A
4.1.8	Interconnect integrity		P
4.1.8.1	Protection from electromagnetic interference		P
	The interconnection system shall have the capability to withstand electromagnetic interference (EMI) environments in accordance with IEEE Std C37.90.2-1995. The influence of EMI shall not result in a change in state or misoperation of the interconnection system.	The interconnection system have the capability to withstand electromagnetic interference (EMI).	P
4.1.8.2	Surge withstand performance		P
	The interconnection system shall have the capability to withstand voltage and current surges in accordance with the environments defined in IEEE Std C62.41.2-2002 or IEEE Std C37.90.1-2002 as applicable.		P
4.1.8.3	Paralleling device		P
	The interconnection system paralleling-device shall be capable of withstanding 220% of the interconnection system rated voltage.		P
4.2	**Response to Area EPS abnormal conditions**		**P**
	Abnormal conditions can arise on the Area EPS that require a response from the connected DR. This response contributes to the safety of utility maintenance personnel and the general public, as well as the avoidance of damage to connected equipment, including the DR. All voltage and frequency parameters specified in these subclauses shall be met at the PCC, unless otherwise stated.	Response contributed to the safety of utility maintenance personnel and the general public as well as the avoidance of damage to connected equipment.	P
4.2.1	Area EPS faults		P
	The DR unit shall cease to energize the Area EPS for faults on the Area EPS circuit to which it is connected.	The unit ceased to energize the Area EPS.	P
4.2.2	Area EPS reclosing coordination		P

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Clause	Requirement – Test	Result – Remark	Verdict
	The DR shall cease to energize the Area EPS circuit to which it is connected prior to reclosure by the Area EPS.		P
4.2.3	Voltage		P
	When any voltage is in a range given in Table 1, the DR shall cease to energize the Area EPS within the clearing time as indicated. Under mutual agreement between the EPS and DR operators, other static or dynamic voltage and clearing time trip settings shall be permitted. Clearing time is the time between the start of the abnormal condition and the DR ceasing to energize the Area EPS. For DR less than or equal to 30 kW 300 W in peak capacity, the voltage set points and clearing times shall be either fixed or field adjustable. For DR greater than 30 kW 300 W, the voltage set points and clearing times shall be field adjustable.	The protection functions of the interconnection system detected the effective of fundamental frequency value of each phase to phase voltage.	P
	The voltages shall be detected at either the PCC or the point of DR connection when any of the following conditions exist:		P
	a) The aggregate capacity of DR systems connected to a single PCC is less than or equal to 30 kW,		P
	b) The interconnection equipment is certified to pass a non-islanding test for the system to which it is to be connected,		P
	c) The aggregate DR capacity is less than 50% of the total Local EPS minimum annual integrated electrical demand for a 15 minute time period, and export of real or reactive power by the DR to the Area EPS is not permitted.		P
	Table 1—Interconnection system default response to abnormal voltages		-
4.2.4	Frequency		P
	When the system frequency is in a range given in Table 2, the DR shall cease to energize the Area EPS within the a pre-set clearing time as indicated. Under mutual agreement between the EPS and DR operators, other static or dynamic frequency and clearing time trip settings shall be permitted. Clearing time is the time between the start of the abnormal	Complied with Table 2.	P

Default settings[a]		
Voltage range (% of base voltage[b])	Clearing time (s)	Clearing time: adjustable up to and including (s)
V < 45	0.16	0.16
45 ≤ V < 60	1	11
60 ≤ V < 88	2	21
110 < V < 120	1	13
V ≥ 120	0.16	0.16

[a] Under mutual agreement between the EPS and DR operators, other static or dynamic voltage and clearing time trip settings shall be permitted

[b] Base voltages are the nominal system voltages stated in ANSI C84.1-2011, Table 1.

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Clause	Requirement – Test	Result – Remark	Verdict
	condition and the DR ceasing to energize the Area EPS.		
	The frequency and time set points in Table 2 shall be field adjustable. Adjustable under-frequency (UF) and over-frequency (OF) trip settings shall be coordinated with the Area EPS operatortions. DR settings for frequency response shall be coordinated with load shedding schemes of the Area EPS.		P
	As mutually agreed upon by the Area EPS and DR operators, DR shall be permitted to provide modulated power output as a function of frequency in coordination with functions UF1,UF2, OF1, and OF2. Operating parameters shall be specified when this function is provided.		N/A
	Table 2—Interconnection system default response to abnormal frequencies Default settings / Ranges of adjustability Function: Frequency (Hz) / Clearing time (s) / Frequency (Hz) / Clearing time (s) adjustable up to and including UF1: < 57 / 0.16 / 56 – 60 / 10 UF2: < 59.5 / 2 / 56 – 60 / 300 OF1: > 60.5 / 2 / 60 – 64 / 300 OF2: > 62 / 0.16 / 60 – 64 / 10		-
4.2.5	Loss of synchronism		N/A
	Loss of synchronism protection is not required except as necessary to meet 4.3.2.		N/A
4.2.6	Reconnection to Area EPS		P
	After an Area EPS disturbance, no DR reconnection shall take place until the Area EPS voltage is within Range B of ANSI C84.1-1995,Table 1, and frequency range of 59.3 Hz to 60.5Hz.		P
	The DR interconnection system shall include an adjustable delay (or a fixed delay of five minutes)that may delay reconnection for up to five minutes after the Area EPS steady-state oltage and frequency are restored to the ranges identified above.		P
4.3	**Power quality**		**P**
4.3.1	Limitation of dc injection		P
	The DR and its interconnection system shall not inject dc current greater than 0.5% of the full rated output current at the point of DR connection.		P
4.3.2	Limitation of flicker induced by the DR		P
	The DR shall not create objectionable flicker for other customers on the Area EPS		P
4.3.3	Harmonics		P
	When the DR is serving balanced linear loads, harmonic current injection into the Area EPS at the PCC shall not exceed the limits stated below in Table 3. The harmonic current injections shall	Complied with specified Table 3.	P

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Clause	Requirement – Test	Result – Remark	Verdict
	be exclusive of any harmonic currents due to harmonic voltage distortion present in the Area EPS without the DR connected.		
	Table 3—Maximum harmonic current distortion in percent of current (I)[a] Individual harmonic order h (odd harmonics)[b] / h < 11 / 11 ≤ h < 17 / 17 ≤ h < 23 / 23 ≤ h < 35 / 35 ≤ h / Total demand distortion (TDD) Percent (%) / 4.0 / 2.0 / 1.5 / 0.6 / 0.3 / 5.0 [a] I = the greater of the Local EPS maximum load current integrated demand (15 or 30 minutes) without the DR unit, or the DR unit rated current capacity (transformed to the PCC when a transformer exists between the DR unit and the PCC). [b] Even harmonics are limited to 25% of the odd harmonic limits above.		-
4.4	Islanding		P
4.4.1	Unintentional islanding		P
	For an unintentional island in which the DR Energizes a portion of the Area EPS through the PCC, the DR interconnection system shall detect the island and cease to energize the Area EPS within two seconds of the formation of an island	DR interconnection system detected the island and cease to energize the Area EPS with two seconds.	P
4.4.2	Intentional islanding		N/A
	This topic is under consideration for future revisions of this standard.		N/A
5	**Interconnection test specifications and requirements**		**P**
	This clause provides the test requirements to demonstrate that the interconnection system meets the requirements of Clause 4. The applicable tests from this clause are required for all interconnection systems. The results of these tests shall be formally documented.		-
	The stated test specifications and requirements are universally needed for interconnection of DR including synchronous machines, induction machines, or static power inverters/converters, and will be sufficient for most installations.		-
5.1	**Design test**		**P**
	This design test shall be performed as applicable to the specific interconnection system technology. The test shall be performed on a representative sample, either in the factory, at a testing laboratory, or on equipment in the field.		-
	This test applies to a packaged interconnection system using embedded components or to an interconnection system that uses an assembly of discrete components.	Considered.	P
	The design test shall be conducted on the same sample in the sequence of Table 4.	The design test was conducted according to Table 4.	P

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Clause	Requirement – Test	Result – Remark	Verdict

	Table 4—Sequence for conducting design test **Required order** / **Design test clause and title** 1 — 5.1.1 Response to abnormal voltage and frequency 2 — 5.1.2 Synchronization 3 — 5.1.3 Interconnect integrity test **Suggested order** 4 — 5.1.1 Response to abnormal voltage and frequency 5 — 5.1.2 Synchronization 6 — 5.1.4 Unintentional islanding 7 — 5.1.5 Limitation of dc injection 8 — 5.1.6 Harmonics		-
5.1.1	Response to abnormal voltage and frequency		P
	This test shall demonstrate that the DR ceases to energize the Area EPS when the voltage or frequency exceeds the limits as specified in 4.2.3 and 4.2.4. Interconnection systems provided with field adjustable set points shall also be tested at the minimum, midpoint, and maximum of the adjustable set point ranges. These tests shall be conducted using either the simulated utility or secondary injection method.		P
5.1.2	Synchronization		P
	Test results conforming to requirements of A, B, or C below are accepted as indicating compliance with the requirements of 4.1.3. The appropriate conditions to be met for specific interconnection system technology follow.		P
A.	Synchronous interconnection to an EPS, or an energized local EPS to an energized Area EPS		N/A
	This test shall demonstrate that at the moment of the paralleling-device closure, all three parameters in Table 5 are within the stated ranges. This test shall also demonstrate that if any of the parameters are outside of the ranges stated in the table, the paralleling-device shall not close.		N/A
B.	Induction interconnection		N/A
	Self-excited induction generators shall be tested as per A in 5.1.2.		N/A
	This test shall determine the maximum start-up (in-rush) current drawn by the unit. The results shall be used, along with Area EPS impedance information for the proposed location, to estimate the starting voltage		N/A

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Clause	Requirement – Test	Result – Remark	Verdict

	Table 5—Synchronization parameter limits for synchronous interconnection to an EPS, or an energized local EPS to an energized Area EPS Aggregate rating of DR units (kVA) / Frequency difference (Δf, Hz) / Voltage difference (ΔV, %) / Phase angle difference (ΔΦ, °) 0 – 500 / 0.3 / 10 / 20 > 500 – 1 500 / 0.2 / 5 / 15 > 1 500 – 10 000 / 0.1 / 3 / 10 drop and verify that the unit shall not exceed the synchronization requirements in 4.1.3 and the flicker requirements in 4.3.2.		
C	Inverter interconnection		P
	An inverter-based interconnection system that produces fundamental voltage before the paralleling device is closed shall be tested according to the procedure for synchronous interconnection as stated in A of 5.1.2.		P
	All other inverter-based interconnection systems shall be tested to determine the maximum start-up current. The results shall be used, along with Area EPS impedance for the proposed location, to estimate the starting voltage magnitude change and verify that the unit shall meet the synchronization requirements in 4.1.3 and the flicker requirements in 4.3.2.		N/A
5.1.3	Interconnect integrity test		P
5.1.3.1	Protection from EMI		P
	The interconnection system shall be tested in accordance with IEEE Std C37.90.2-1995 to confirm that the results are in compliance with 4.1.8.1. The influence of EMI shall not result in a change in state or mis-operation of the interconnection system.	Refer to report No. ENS2308010128E00101R, tested and issued by EMTEK (SHENZHEN) CO., LTD., dated on 15 August 2023.	P
5.1.3.2	Surge withstand performance		P
	The interconnection system shall be tested for the requirement in 4.1.8.2 in all normal operating modes in accordance with IEEE Std C62.45-2002 for equipment rated less than 1000 V to confirm that the surge withstand capability is met by using the selected test level(s) from IEEE Std C62.41.2-2002. Interconnection system equipment rated greater than 1000 V shall be tested in accordance with manufacturer or system integrator designated applicable standards. For interconnection system equipment signal and control circuits, use IEEE Std C37.90.1-2002. The results	Surge test is under 6kV	P
5.1.3.3	Paralleling device		P
	A dielectric test across the open-circuited paralleling device shall be conducted to confirm compliance with the requirements of 4.1.8.3.	Dielectric test is under 2000Va.c.	P
5.1.4	Unintentional Islanding		P
	A test or field verification shall be conducted to confirm that 4.4.1 is met regardless of the selected		P

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Clause	Requirement – Test	Result – Remark	Verdict
	method of detecting isolation.		
5.1.5	Limitation of dc injection		P
	Inverter based DR shall be tested to confirm that the DR does not inject dc current greater than prescribed limits that are listed in 4.3.1.		P
5.1.6	Harmonics		P
	The intent of the harmonics interconnection test is to assess that under a controlled set of conditions the DR unit meets the harmonic limits specified in 4.3.3.		P
	The DR shall be operated in parallel with a predominantly inductive voltage source with a short circuit current capacity ISC of not less than 20 times the DR rated output current at fundamental frequency. The voltage and frequency output of the voltage source shall correspond to the rated voltage and frequency of the DR. The unloaded voltage waveform produced by the Area EPS or simulated utility voltage source shall have a total harmonic distortion (THD) less than 2.5%.		P
	The DR shall be operated at an output test load current, IL, of 33%, 66%, and at a level as close to 100% of rated output current as practical. Use total rated-current distortion (TRD) in place of TDD. TRD is the total rms value of the sum of the current harmonics created by the DR unit operating into a linear balanced load divided by the greater of the test load current (IL) demand or the rated current capacity of the DR unit (Irated). The individual harmonic distortion and TRD of the DR output current shall be measured for the first 40 harmonics. The harmonic current injections shall be exclusive of any harmonic currents due to harmonic voltage distortion present in the Area EPS without the DR connected. The test results shall not exceed the values in 4.3.3, Table 3.	The unit has operated at an output test load 33%, 66% and at a level as close to100%	P
	As an alternative, a synchronous generator DR shall be tested to meet the requirements of 4.3.3; either after installation or while powering a balanced resistive load and isolated from any other sources. The voltage harmonics while powering a resistive load at 100% of the machine kVA rating shall not exceed the levels in Table 6. Voltage harmonics shall be measured line to line for 3-phase/3 wire systems, and line to neutral for 3-phase/4-wire systems.		N/A
	Table 6—Maximum harmonic voltage distortion in percent of rated voltage for synchronous machines Individual harmonic order: h < 11 | 11 ≤ h < 17 | 17 ≤ h < 23 | 23 ≤ h < 35 | 35 ≤ h | Total harmonic distortion Percent (%): 4.0 | 2.0 | 1.5 | 0.6 | 0.3 | 5.0		

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Clause	Requirement – Test	Result – Remark	Verdict
5.2	**Production tests**		N/A
	Each interconnection system shall be subjected to requirements of 5.1.1 and 5.1.2. Interconnection systems with adjustable set points shall be tested at a single set of set points as specified by the manufacturer. This test may be conducted as a factory test or may be performed as part of a commissioning test (see 5.4)**.**	Considered by the manufacturer during production	N/A
5.3	**Interconnection installation evaluation**		**N/A**
5.3.1	Grounding integration with Area EPS		N/A
	A system design verification shall be made to ensure that the requirements of 4.1.2 have been met.		N/A
5.3.2	Isolation device		N/A
	A system design verification shall be made to ensure that the requirements of 4.1.7 have been met.		N/A
5.3.3	Monitoring provisions		N/A
	A system design verification shall be made to ensure that the provisions for monitoring are in accordance with 4.1.6.		N/A
5.3.4	Area EPS faults		N/A
	A system design verification shall be made to ensure that the requirements of 4.2.1 have been met.		N/A
5.3.5	Area EPS reclosing coordination		N/A
	A system design verification shall be made to verify the interconnection system is coordinated with the Area EPS reclosing practices in accordance with 4.2.2.		N/A
5.4	**Commissioning tests**		N/A
	All commissioning tests shall be performed based on written test procedures.19 The following visual inspections shall be performed.		N/A
	— A visual inspection shall be made to ensure that the grounding coordination requirement of 4.1.2 has been implemented. — A visual inspection shall be made to confirm the presence of the isolation device if required by 4.1.7.		N/A
	Initial commissioning tests shall be performed on the installed DR and interconnection system equipment prior to the initial parallel operation of the DR. The following tests are required:		N/A
	— Operability test on the isolation device — Unintentional-islanding functionality as specified in 5.4.1 — Cease to energize functionality as specified in 5.4.2 — Any tests of 5.1 that have not been previously performed on a representative sample and formally		N/A

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Clause	Requirement – Test	Result – Remark	Verdict
	documented — Any tests of 5.2 that have not been previously performed		
	The applicable tests of 5.1 shall be repeated when:		N/A
	— Functional software or firmware changes have been made on the interconnection system — Any hardware component of the interconnection system has been modified in the field, or, replaced or repaired with parts different from the tested configuration.	Manufactuer has control and procedure to verify changes software or firmware.	N/A
	Sublauses 5.4.1 and 5.4.2, and the applicable tests of 5.2 shall be repeated if:		N/A
	— Protection settings have been changed after factory testing. — Protection functions have been adjusted after the initial commissioning process.		N/A
5.4.1	Unintentional islanding functionality test		N/A
5.4.1.1	Reverse-power or minimum power test		N/A
	A reverse-power or minimum power function, if used to meet the requirements of 4.4.1, shall be tested using injection techniques or by adjusting the DR output and local loads to verify that the reverse power or minimum power function is met.		N/A
5.4.1.2	Non-islanding functionality test		N/A
	For non-islanding interconnection systems, 5.4.2 satisfies this requirement.		N/A
5.4.1.3	Other unintentional islanding functionality tests		N/A
	If tests in 5.4.1.1 and 5.4.1.2 are not applicable to the interconnection system, the interconnection system shall be tested in accordance with procedures provided by the manufacturer or system integrator.		N/A
5.4.2	Cease to energize functionality test		N/A
	Check the cease to energize functionality by operating a load interrupting device and verify the equipment ceases to energize its output terminals and does not restart/reconnect for the required time delay. The test shall be performed on each phase individually. This test verifies conformance to the cease to energize requirement of 4.1.4, 4.2.1, 4.2.2, 4.2.3, 4.2.4, and 4.4.1.		N/A
5.5	**Periodic interconnection tests**		**N/A**
	All interconnection-related protective functions and associated batteries shall be periodically tested at intervals specified by the manufacturer, system integrator, or the authority who has jurisdiction over the DR interconnection. Periodic test reports or a log for inspection shall be maintained.		N/A

Testing Result

4.1.8	Interconnect integrity	P

Performance Criterion:

A - operate as intended during and after the test
B - operate as intended after the test
C - loss/error of function

Required Criterion: B

☑ For IEEE Std C62.41.2 ™ -2002

Test Port	Applied Voltage (kV)	Repetition Frequency (kHz)	Result
A.C. Power supply line	±4kV	2.5k	A

☑ For IEEE Std C37.90.1 ™ -2002

Test Port	Applied Voltage (kV)	Repetition Frequency (kHz)	Result
D.C. Power supply line	±4kV	2.5k	A
External signal and control circuits	±4kV	2.5k	A

Performance Criterion:

A - operate as intended during and after the test
B - operate as intended after the test
C - loss/error of function

Required Criterion: B

Test Port	Applied Voltage (kV)	Result
A.C. Power supply line	Line to line ±6kV	A
A.C. Power supply line	line to earth ±6kV	A

Testing Result

5.2	Test for response to abnormal voltage conditions (25℃)						P
Testing item	Tripping voltage/ Clearing time setting	Measured Tripping voltage/ Clearing time					
		Phase	1	2	3	4	5
Voltage - under (<45%)	101.2V/ 0.16s	L-N	100.15V/ 0.131s	100.28V/ 0.141s	100.24V/ 0.124s	100.37V/ 0.137s	100.39V/ 0.133s
Voltage - under (<60%)	135.7V/ 1s	L-N	133.75V/ 0.988 s	134.01V/ 0.985s	133.89V/ 0.979s	133.76V/ 0.980s	133.77V/ 0.972s
	135.7V/ 6s	L-N	134.21V/ 5.975s	134.30V/ 6.000s	133.94V/ 5.943s	133.85V/ 5.988s	133.84V/ 5.979s
	135.7V/11s	L-N	134.10V/ 10.985s	133.75V/ 11.000s	133.79V/ 11.121s	133.92V/ 10.997s	134.11V/ 11.005s
Voltage - under (<88%)	200.1V/ 2s	L-N	197.56V/ 1.975s	197.54V/ 1.980s	196.45V/ 1.972s	196.87V/ 1.985s	196.91V/ 1.989s
	200.1V / 11.5s	L-N	197.43V/ 11.500s	197.80V/ 11.450s	197.96V/ 11.486s	197.77V/ 11.463s	198.25V/ 11.471s
	200.1V / 21s	L-N	197.50V/ 21.000s	197.83V/ 21.000s	197.94V/ 21.027s	198.01V/ 20.984s	197.53V/ 20.990s
Voltage – over (>110%)	253V/ 1s	L-N	249.64V/ 0.970s	249.70V/ 0.988s	249.43/ 0.973s	249.49V/ 0.980s	249.41V/ 0.986s
	253V/ 7s	L-N	249.31V/ 6.985s	249.33V/ 6.985s	249.60V/ 6.988s	249.89V/ 6.991s	249.71V/ 6.990s
	253V/ 13s	L-N	249.87V/ 12.980s	249.72V/ 12.980s	249.65V/ 12.982s	249.49V/ 12.986s	249.63V/ 12.979s
Voltage – over (≥120%)	276V/ 0.16s	L-N	272.92V/ 0.144s	272.93V/ 0.133s	272.90V/ 0.148s	272.92V/ 0.137s	272.81V/ 0.140s
Remark: Same evalution after EMC test and Dielectric test							

Testing Result

5.2	Test for response to abnormal voltage conditions (-25℃)						P
Testing item	Tripping voltage/ Clearing time setting	Measured Tripping voltage/ Clearing time					
		Phase	1	2	3	4	5
Voltage - under (<45%)	101.2V/ 0.16s	L-N	97.96V/ 0.157s	98.01V/ 0.159s	97.99V/ 0.156s	98.00V/ 0.157s	97.98V/ 0.160s
Voltage - under (<60%)	135.7V/ 1s	L-N	133.06V/ 0.968s	133.10V/ 0.962s	133.08V/ 0.963s	133.08V/ 0.972s	133.11V/ 0.976s
	135.7V/ 6s	L-N	133.08V/ 6.033s	133.09V/ 5.998s	133.12V/ 6.029s	133.10V/ 6.027s	133.09V/ 6.030s
	135.7V/11s	L-N	133.09V/ 10.980s	133.07V/ 10.984s	133.06V/ 10.991s	133.10V/ 10.987s	133.11V/ 10.986s
Voltage - under (<88%)	200.1V/ 2s	L-N	197.98V/ 1.986s	197.99V/ 1.997s	197.98V/ 1.980s	197.97V/ 1.989s	197.96V/ 1.995s
	200.1V / 11.5s	L-N	197.94V/ 11.462s	197.98V/ 11.470s	197.95V/ 11.469s	197.98V/ 11.485s	197.99V/ 11.482s
	200.1V / 21s	L-N	197.98V/ 22.671s	197.95V/ 20.970s	197.97V/ 20.966s	197.96V/ 20.966s	197.99V/ 20.979s
Voltage – over (>110%)	253V/ 1s	L-N	251.73V/ 0.968s	251.82V/ 0.973s	253.1.75V/ 0.969s	251.74V/ 0.985s	251.76V/ 0.969s
	253V/ 7s	L-N	251.95V/ 6.978s	251.98V/ 6.980s	251.95V/ 6.9100s	251.94V/ 6.982s	251.97V/ 6.958
	253V/ 13s	L-N	251.98V/ 12.964s	251.96V/ 12.973s	251.98V/ 12.979s	251.97V/ 12.953s	251.94V/ 12.964s
Voltage – over (≥120%)	276V/ 0.16s	L-N	274.60V/ 0.131s	274.64V/ 0.148s	274.74V/ 0.142s	274.67V/ 0.133s	274.64V/ 0.139s

Testing Result

5.2	Test for response to abnormal voltage conditions (60℃)						P
Testing item	Tripping voltage/ Clearing time setting	Measured Tripping voltage/ Clearing time					
		Phase	1	2	3	4	5
Voltage - under (<45%)	101.2V/ 0.16s	L-N	100.55V/ 0.136s	100.54V/ 0.137s	100.56V/ 0.139s	100.55V/ 0.137s	100.57V/ 0.140s
Voltage - under (<60%)	135.7V/ 1s	L-N	132.09V/ 0.956s	132.08V/ 0.985s	132.10V/ 0.958s	132.09V/ 0.974s	132.10V/ 0.991s
	135.7V/ 6s	L-N	132.08V/ 5.974s	132.09V/ 5.962s	132.10V/ 5.964s	132.11V/ 5.968s	132.09V/ 5.973s
	135.7V/11s	L-N	132.09V/ 11.013s	132.08V/ 10.971s	132.10V/ 10.975s	132.10V/ 10.987s	132.09V/ 10.982s
Voltage - under (<88%)	200.1V/ 2s	L-N	197.29V/ 1.970s	197.34V/ 1.976s	197.53V/ 1.983s	197.52V/ 1.973s	197.43V/ 1.975s
	200.1V / 11.5s	L-N	196.56V/ 11.480s	196.56V/ 11.484s	196.55V/ 11.471s	196.54V/ 11.489s	195.56V/ 11.476s
	200.1V / 21s	L-N	196.58V/ 20.968s	196.60V/ 20.966s	196.58V/ 20.968s	196.59V/ 20.977s	196.58V/ 20.973s
Voltage – over (>110%)	253V/ 1s	L-N	249.37V/ 0.980s	249.40V/ 0.979s	249.39V/ 0.983s	249.40V/ 0.991s	249.38V/ 0.988s
	253V/ 7s	L-N	249.50V/ 6.970s	249.49V/ 6.979s	249.48V/ 6.974s	249.46V/ 6.986s	249.49V/ 6.975s
	253V/ 13s	L-N	249.51V/ 12.955s	249.48V/ 12.967s	249.47V/ 12.974s	249.50V/ 12.964s	240.51V/ 12.959s
Voltage – over (≥120%)	276V/ 0.16s	L-N	272.90V/ 0.121s	272.81/ 0.125s	272.79V/ 0.120s	272.931V/ 0.120s	272.92V/ 0.118s

Testing Result

5.3	Response to abnormal frequency conditions (25℃)					P
Testing item	Tripping frequency/ Clearing time setting	Measured Tripping frequency/ Clearing time				
		1	2	3	4	5
Frequency - under UF1	56.00Hz/ 0.16s	55.790Hz/ 0.140s	55.820Hz/ 0.149s	55.840Hz/ 0.144s	55.800Hz/ 0.147s	55.810Hz/ 0.149s
Frequency - under UF1	58.00Hz/ 5s	57.810Hz/ 4.983s	57.800Hz/ 4.959s	57.820Hz/ 4.987s	57.810Hz/ 4.964s	57.800Hz/ 4.970s
Frequency - under UF1	59.50Hz/ 10s	59.470Hz/ 9.976s	59.480Hz/ 9.963s	59.480Hz/ 9.969s	59.470Hz/ 9.983s	59.470Hz/ 9.960s
Frequency - under UF2	56.00Hz/ 2s	55.800Hz/ 1.974s	55.830Hz/ 1.982s	55.790Hz/ 1.985s	55.810Hz/ 1.987s	55.820Hz/ 1.989s
Frequency - under UF2	58.00Hz/ 151s	57.820Hz/ 150.977s	57.800Hz/ 150.980s	57.820Hz/ 150.986s	57.810Hz/ 150.983s	57.830Hz/ 150.979s
Frequency - under UF2	59.50Hz/ 300s	59.478Hz/ 299.970s	59.474Hz/ 299.875s	59.480Hz/ 299.972s	59.783Hz/ 299.988s	59.4820Hz/ 299.984s
Frequency - over OF1	60.50Hz/ 2s	60.500Hz/ 1.981s	60.594Hz/ 1.985s	60.593Hz/ 1.983s	60.593Hz/ 1.991s	60.600Hz/ 1.986s
Frequency - over OF1	62.00Hz/ 151s	61.998Hz/ 150.900s	62.008Hz/ 150.511s	62.008Hz/ 150.737s	62.009Hz/ 150.875s	61.993Hz/ 150.892s
Frequency - over OF1	64.00Hz/ 300s	64.006Hz/ 299.988s	64.005Hz/ 299.978s	64.018Hz/ 299.978s	64.005Hz/ 299.982s	64.003Hz/ 299.989s
Frequency - over OF2	60.50Hz/ 0.16s	60.581Hz/ 0.150s	60.573Hz/ 0.148s	60.575Hz/ 0.148s	60.582Hz/ 0.152s	60.568Hz/ 0.149s
Frequency - over OF2	62.00Hz/ 5s	62.004Hz/ 4.980s	61.994Hz/ 4.983s	62.007Hz/ 4.981s	62.001Hz/ 4.979s	62.003Hz/ 4.987s
Frequency - over OF2	64.00Hz/ 10s	64.002Hz/ 9.957s	64.004Hz/ 9.972s	63.998Hz/ 9.979s	64.001Hz/ 9.962s	64.001Hz/ 9.975s
Remark: Same evaluation after EMC test and Dielectric test						

Testing Result

5.3	Response to abnormal frequency conditions (-25℃)					P
Testing item	Tripping frequency/ Clearing time setting	Measured Tripping frequency/ Clearing time				
		1	2	3	4	5
Frequency - under UF1	56.00Hz/ 0.16s	55.910Hz/ 0.148s	55.900Hz/ 0.149s	55.912Hz/ 0.149s	55.911Hz/ 0.146s	55.912Hz/ 0.147s
Frequency - under UF1	58.00Hz/ 5s	57.910Hz/ 4.997s	57.912Hz/ 4.987s	57.910Hz/ 4.985s	57.911Hz/ 4.994s	57.911Hz/ 4.979s
Frequency - under UF1	59.50Hz/ 10s	59.380Hz/ 9.981s	59.381Hz/ 9.974s	59.381Hz/ 9.972s	59.380Hz/ 9.980s	59.382Hz/ 9.976s
Frequency - under UF2	56.00Hz/ 2s	55.912Hz/ 1.994s	55.910Hz/ 1.981s	55.913Hz/ 1.987s	55.910Hz/ 1.978s	55.911Hz/ 1.980s
Frequency - under UF2	58.00Hz/ 151s	57.961Hz/ 150.984s	57.961Hz/ 150.985s	57.959Hz/ 151.000s	57.961Hz/ 150.983s	57.958Hz/ 150.972s
Frequency - under UF2	59.50Hz/ 300s	59.383Hz/ 299.982s	59.382Hz/ 299.968s	59.381Hz/ 299.986s	59.380Hz/ 299.985s	59.382Hz/ 299.987s
Frequency - over OF1	60.50Hz/ 2s	60.610Hz/ 1.970s	60.611Hz/ 1.980s	60.610Hz/ 1.982s	60.611Hz/ 1.982s	60.610Hz/ 1.982s
Frequency - over OF1	62.00Hz/ 151s	62.016Hz/ 151.001s	62.019Hz/ 150.995s	62.019Hz/ 150.989s	62.017Hz/ 150.994s	62.017Hz/ 150.991s
Frequency - over OF1	64.00Hz/ 300s	64.006Hz/ 299.982s	64.005Hz/ 299.974s	64.018Hz/ 299.985s	64.005Hz/ 299.982s	64.013Hz/ 299.979s
Frequency - over OF2	60.50Hz/ 0.16s	60.609Hz/ 0.144s	60.608Hz/ 0.138s	60.610Hz/ 0.138s	60.609Hz/ 0.136s	60.609Hz/ 0.149s
Frequency - over OF2	62.00Hz/ 5s	62.019Hz/ 4.997s	62.019Hz/ 4.974s	62.017Hz/ 4.980s	62.019Hz/ 4.972s	62.020Hz/ 4.972s
Frequency - over OF2	64.00Hz/ 10s	64.011Hz/ 9.977s	64.011Hz/ 9.984s	64.013Hz/ 9.979s	64.014Hz/ 9.986s	64.016Hz/ 9.978s

Testing Result

5.3	Response to abnormal frequency conditions (60℃)					P
Testing item	Tripping frequency/ Clearing time setting	Measured Tripping frequency/ Clearing time				
		1	2	3	4	5
Frequency - under UF1	56.00Hz/ 0.16s	55.981Hz/ 0.146s	55.979Hz/ 0.146s	55.982Hz/ 0.148s	55.981Hz/ 0.150s	55.980Hz/ 0.151s
Frequency - under UF1	58.00Hz/ 5s	57.973Hz/ 4.970s	57.969Hz/ 4.974s	57.968Hz/ 4.973s	57.974Hz/ 4.972s	57.971Hz/ 4.971s
Frequency - under UF1	59.50Hz/ 10s	59.506Hz/ 9.975s	59.507Hz/ 9.977s	59.509Hz/ 9.981s	59.510Hz/ 9.979s	59.509Hz/ 9.976s
Frequency - under UF2	56.00Hz/ 2s	55.982Hz/ 1.985s	55.984Hz/ 1.988s	55.987Hz/ 1.986s	55.975Hz/ 1.990s	55.984Hz/ 1.986s
Frequency - under UF2	58.00Hz/ 151s	57.983Hz/ 150.973s	57.979Hz/ 150.974s	57.983Hz/ 150.976s	57.974Hz/ 150.972s	57.980Hz/ 150.981s
Frequency - under UF2	59.50Hz/ 300s	59.511Hz/ 299.980s	59.512Hz/ 299.981s	59.510Hz/ 299.984s	59.509Hz/ 299.989s	59.508Hz/ 299.987s
Frequency - over OF1	60.50Hz/ 2s	60.590Hz/ 1.978s	60.585Hz/ 1.979s	60.585Hz/ 1.985s	60.589Hz/ 1.976s	60.591Hz/ 1.984s
Frequency - over OF1	62.00Hz/ 151s	62.001Hz/ 150.974s	62.002Hz/ 150.983s	62.000Hz/ 150.977s	62.004Hz/ 150.975s	62.007Hz/ 150.979s
Frequency - over OF1	64.00Hz/ 300s	64.006Hz/ 299.980s	64.005Hz/ 299.985s	64.018Hz/ 299.981s	64.005Hz/ 299.989s	64.013Hz/ 299.982s
Frequency - over OF2	60.50Hz/ 0.16s	60.593Hz/ 0.145s	60.592Hz/ 0.131s	60.592Hz/ 0.136s	60.596Hz/ 0.138s	60.590Hz/ 0.137s
Frequency - over OF2	62.00Hz/ 5s	62.003Hz/ 4.985s	62.004Hz/ 4.973s	62.001Hz/ 4.978s	62.004Hz/ 4.981s	62.003Hz/ 4.978s
Frequency - over OF2	64.00Hz/ 10s	64.006Hz/ 9.972s	64.004Hz/ 9.973s	64.004Hz/ 9.981s	64.002Hz/ 9.984s	64.003Hz/ 9.983s

Testing Result

5.4.4	Startup current measurement (Method 2)			P
1	2	3	4	5
13.4A	13.4A	13.9A	13.5A	13.2A
6	7	8	9	10
13.9A	14.1A	14.3A	13.8A	13.4A

5.5.3	Dielectric test	P
Applied points:	Applied voltage:	Breakdown or flashover?
Between Input and output	2000V	No

5.6	DC Injection for inverters without interconnection transformers		P
Rated output load:	10kW	33 % of rated output load:	3.33kW
Output voltage:	230.53V	Output current (rms)	14.073A
DC current:	0.063A/0.14%	DC current limit	0.5%In
Rated output load:	10Kw	66 % of rated output load:	6.67kW
Output voltage:	230.86V	Output current (rms)	24.393A
DC current:	0.081A/0.19%	DC current limit	0.5%In
Rated output load:	10kW	100 % of rated output load:	10kW
Output voltage:	231.45V	Output current (rms)	40.859A
DC current:	0.029A/0.07%	DC current limit	0.5%In
Model: SUN2000-10K-LC0			

Testing Result

5.7.1	Unintentional islanding test			P
Initial State with 100% Load				
	Q (VAR)	**Voltage**	**Watt**	**VA**
R Load	--	230.18V	9.96kW	--
L Load	9.95kVar	230.18V	--	--
C Load	9.96kVar	230.18V	--	--
Islanding Test with 100% Load				
Q(VAR)	**Voltage**	**Watt**	**VA**	**Trip time (ms)**
-5%	230.1V	9.96kW	--	234.318
-4%	230.1V	9.96kW	--	254.915
-3%	230.1V	9.96kW	--	261.794
-2%	230.1V	9.96kW	--	269.297
-1%	230.1V	9.96kW	--	331.442
0%	230.1V	9.96kW	--	419.022
1%	230.1V	9.96kW	--	368.729
2%	230.1V	9.96kW	--	274.224
3%	230.1V	9.96kW	--	265.835
4%	230.1V	9.96kW	--	261.307
5%	230.1V	9.96kW	--	246.659

Islanding Test with 100% Load			
Q(VAR)	**Trip time (ms)**		**Limit**
	the second time	**the third time**	
-1%	336.188	343.588	< 2 s
0%	437.529	481.146	< 2 s
1%	387.714	359.078	< 2 s

Testing Result

5.7.1	Unintentional islanding test			P
Initial State with 66% Load				
	Q (VAR)	**Voltage**	**Watt**	**VA**
R Load	--	229.80V	6.56kW	--
L Load	6.58kVar	229.80V	--	--
C Load	6.57kVar	229.80V	--	--
Islanding Test with 66% Load				
Q(VAR)	**Voltage**	**Watt**	**VA**	**Trip time (ms)**
-5%	229.80V	6.56kW	--	221.579
-4%	229.80V	6.56kW	--	270.540
-3%	229.80V	6.56kW	--	295.132
-2%	229.80V	6.56kW	--	299.793
-1%	229.80V	6.56kW	--	340.897
0%	229.80V	6.56kW	--	394.519
1%	229.80V	6.56kW	--	350.529
2%	229.80V	6.56kW	--	310.535
3%	229.80V	6.56kW	--	299.659
4%	229.80V	6.56kW	--	288.429
5%	229.80V	6.56kW	--	254.737

Islanding Test with 66% Load			
Q(VAR)	**Trip time(ms)**		**Limit**
	the second time	**the third time**	
-1%	349.382	352.741	< 2 s
0%	400.459	409.965	< 2 s
1%	373.321	369.624	< 2 s

Testing Result

5.7.1	Unintentional islanding test			P
Initial State with 33% Load				
	Q (VAR)	**Voltage**	**Watt**	**VA**
R Load	--	229.90V	3.30kW	--
L Load	3.31kVar	229.90V	--	--
C Load	3.31kVar	229.90V	--	--
Islanding Test with 33% Load				
Q(VAR)	**Voltage**	**Watt**	**VA**	**Trip time (ms)**
-5%	229.90V	3.30kW	--	264.769
-4%	229.90V	3.30kW	--	290.293
-3%	229.90V	3.30kW	--	314.219
-2%	229.90V	3.30kW	--	346.889
-1%	229.90V	3.30kW	--	402.021
0%	229.90V	3.30kW	--	487.514
1%	229.90V	3.30kW	--	410.144
2%	229.90V	3.30kW	--	355.412
3%	229.90V	3.30kW	--	315.018
4%	229.90V	3.30kW	--	303.654
5%	229.90V	3.30kW	--	271.428

Islanding Test with 33% Load			
Q(VAR)	**Trip time(ms)**		**Limit**
	the second time	**the third time**	
-1%	410.407	428.431	< 2 s
0%	479.174	482.743	< 2 s
1%	452.578	424.014	< 2 s

Testing Result

5.9	Open phase			P
DC input:	AC output:	Load condition:	Clearing time limit:	
387.43V	229.08	9.84kW	2 sec.	
1	2	3	4	5
63.8ms	57ms	78.4ms	69.00ms	70.8ms
L disconnected				

5.10	Reconnect following abnormal condition disconnect		P
DC input:	AC output:	Load condition:	Re-connect time setting:
389.49V/25.50A/9901.22kW	230.10V/43.30A/9.96W	9.96kW	300s
Overvoltage Verification:			
Overvoltage = 1.15Un	Does the EUT trip? ☑ Yes ☐ No		
Maintain the overvoltage for t > 2 $t_{reconnect}$	Does the EUT reconnect? ☐ Yes ☑ No		
Step change back to the $V_{nominal}$	The reconnect time is 323.4		
Step change back to 1.15Un	Does the EUT reconnect? ☐ Yes ☑ No		
Additional voltage excursion test	Does the EUT reconnect timer reset? ☑ Yes ☐ No		
Undervoltage Verification:			
Undervoltage = 0.83Un	Does the EUT trip? ☑ Yes ☐ No		
Maintain the undervoltage for t > 2 $t_{reconnect}$	Does the EUT reconnect? ☐ Yes ☑ No		
Step change back to the $V_{nominal}$	The reconnect time is 355.26		
Step change back to 0.83Un	Does the EUT reconnect? ☐ Yes ☑ No		
Additional voltage excursion test	Does the EUT reconnect timer reset? ☑ Yes ☐ No		
Overfrequency Verification:			
Overfrequency = 63.5Hz	Does the EUT trip? ☑ Yes ☐ No		
Maintain the frequency for t > 2 $t_{reconnect}$	Does the EUT reconnect? ☐ Yes ☑ No		
Step change back to the $F_{nominal}$	The reconnect time is 324.0		
Step change back to 63.5Hz	Does the EUT reconnect? ☐ Yes ☑ No		
Additional voltage excursion test	Does the EUT reconnect timer reset? ☑ Yes ☐ No		
Underfrequency Verification:			
Underfrequency = 56.5Hz	Does the EUT trip? ☑ Yes ☐ No		
Maintain the underfrequency for t > 2 $t_{reconnect}$	Does the EUT reconnect? ☐ Yes ☑ No		
Step change back to the $F_{nominal}$	The reconnect time is 323.57		
Step change back to 56.5Hz	Does the EUT reconnect? ☐ Yes ☑ No		
Additional voltage excursion test	Does the EUT reconnect timer reset? ☑ Yes ☐ No		

Testing Result

5.11	Harmonics test for inverters								P
Load current: 33 %		EUT rated current: 43.48A				DC input: 387.47Vdc; AC output: 230.31Vac AC output current: 14.10 A			
Harm. order h	1	2	3	4	5	6	7	8	9	10
Harm. (%)		0.114	0.134	0.031	0.202	0.023	0.203	0.024	0.188	0.025
Limit (%)		1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	0.5
Harm. order h	11	12	13	14	15	16	17	18	19	20
Harm. (%)	0.167	0.025	0.126	0.025	0.128	0.023	0.090	0.022	0.091	0.021
Limit (%)	2.0	0.5	2.0	0.5	2.0	0.375	1.5	0.375	1.5	0.375
Harm. order h	21	22	23	24	25	26	27	28	29	30
Harm. (%)	0.063	0.023	0.051	0.022	0.039	0.022	0.033	0.022	0.027	0.031
Limit (%)	1.5	0.15	0.6	0.15	0.6	0.15	0.6	0.15	0.6	0.15
Harm. order h	31	32	33	34	35	36	37	38	39	40
Harm. (%)	0.032	0.022	0.039	0.023	0.043	0.021	0.056	0.023	0.050	0.023
Limit (%)	0.6	0.15	0.6	0.075	0.3	0.075	0.3	0.075	0.3	0.075
TRD (%)						1.163				
Limit (%)						5				

Testing Result

5.11	Harmonics test for inverters									P
Load current: 66 %			EUT rated current: 43.48 A				DC input: 325.00Vdc; AC output: 230.30Vac AC output current: 28.10 A			
Harm. order h	1	2	3	4	5	6	7	8	9	10
Harm. (%)		0.030	0.142	0.156	0.124	0.032	0.102	0.027	0.097	0.023
Limit (%)		1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	0.5
Harm. order h	11	12	13	14	15	16	17	18	19	20
Harm. (%)	0.081	0.024	0.060	0.023	0.085	0.023	0.047	0.022	0.076	0.022
Limit (%)	2.0	0.5	2.0	0.5	2.0	0.375	1.5	0.375	1.5	0.375
Harm. order h	21	22	23	24	25	26	27	28	29	30
Harm. (%)	0.044	0.021	0.065	0.021	0.055	0.022	0.055	0.021	0.060	0.033
Limit (%)	1.5	0.15	0.6	0.15	0.6	0.15	0.6	0.15	0.6	0.15
Harm. order h	31	32	33	34	35	36	37	38	39	40
Harm. (%)	0.050	0.022	0.051	0.022	0.057	0.022	0.038	0.022	0.065	0.023
Limit (%)	0.6	0.15	0.6	0.075	0.3	0.075	0.3	0.075	0.3	0.075
TRD (%)						0.879				
Limit (%)						5				

Testing Result

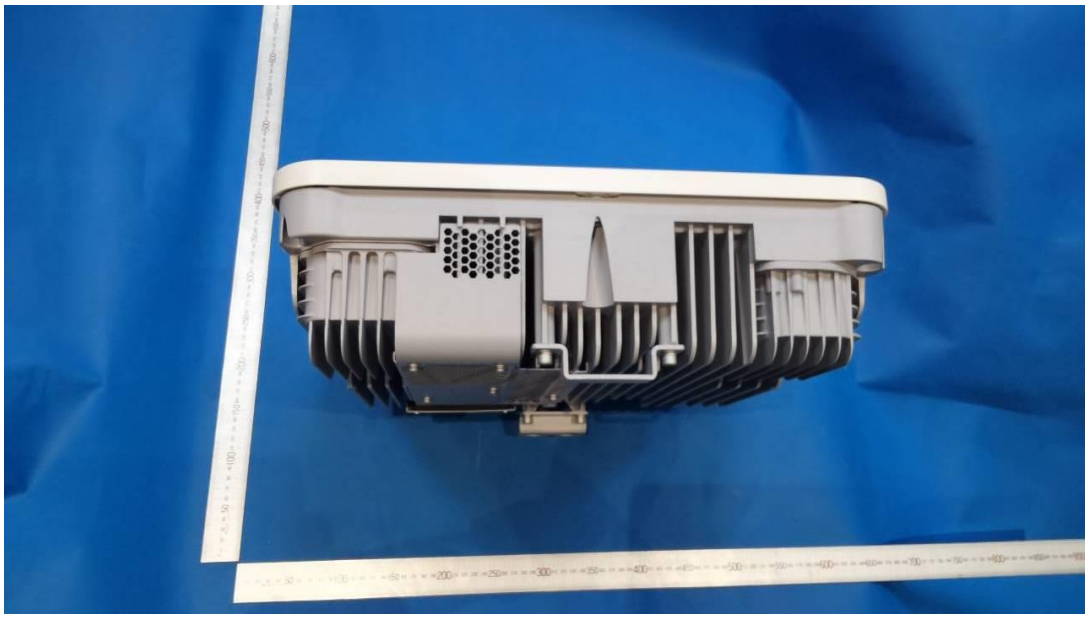
5.11	Harmonics test for inverters								P
Load current: 100 %			EUT rated current: 43.48 A				DC input: 349.71Vdc; AC output:231.21Vac AC output current: 42.87A			
Harm. order h	1	2	3	4	5	6	7	8	9	10
Harm. (%)		0.122	0.422	0.017	0.181	0.027	0.110	0.021	0.063	0.122
Limit (%)		1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	0.5
Harm. order h	11	12	13	14	15	16	17	18	19	20
Harm. (%)	0.020	0.044	0.022	0.041	0.022	0.040	0.036	0.034	0.031	0.030
Limit (%)	2.0	0.5	2.0	0.5	2.0	0.375	1.5	0.375	1.5	0.375
Harm. order h	21	22	23	24	25	26	27	28	29	30
Harm. (%)	0.029	0.025	0.027	0.020	0.025	0.021	0.024	0.017	0.019	0.012
Limit (%)	1.5	0.15	0.6	0.15	0.6	0.15	0.6	0.15	0.6	0.15
Harm. order h	31	32	33	34	35	36	37	38	39	40
Harm. (%)	0.019	0.011	0.017	0.009	0.015	0.006	0.017	0.007	0.017	0.011
Limit (%)	0.6	0.15	0.6	0.075	0.3	0.075	0.3	0.075	0.3	0.075
TRD (%)						1.204				
Limit (%)						5				

Appendix 1: Photos

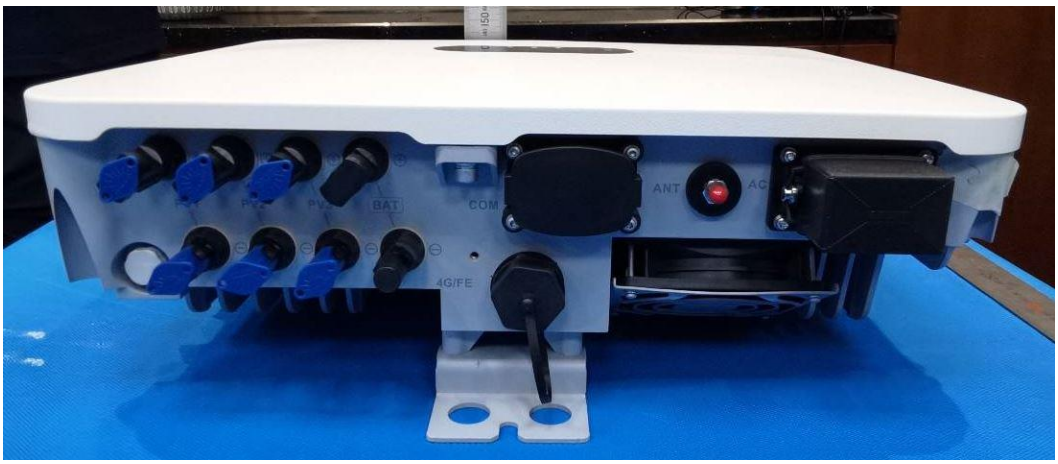
Front view

Side view

Appendix 1: Photos

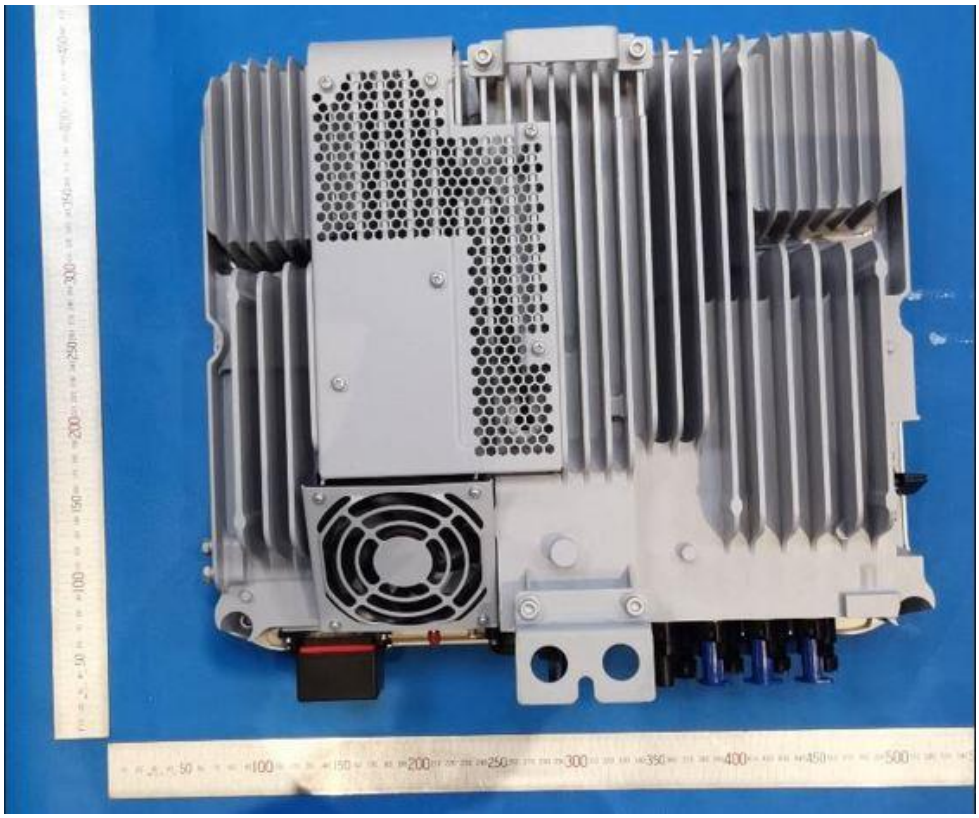


Top view



Connection view

Appendix 1: Photos



Bottom view

(End of Report)